REMARKS

Claims 1, 4-22, 24 and 25 are now present in this application.

Claim 1 has been amended, claims 2 and 3 have been cancelled without prejudice or disclaimer, and claim 25 has been presented. Reconsideration of the application, as amended, is respectfully requested.

Claims 1, 7, 8, 11 and 24 stand rejected under 35 USC 103 as being unpatentable over Bacchetta et al., U.S. Patent 5,627,403, in view of Wu, U.S. Patent 6,689,658. This rejection is respectfully traversed.

Claims 2, 3 and 10 stand rejected under 35 USC 103 as being unpatentable over Bacchetta in view of Wu, and further in view of Higashitani et al., U.S. Patent 6,346,737. This rejection is respectfully traversed.

Claims 4-6 and 10 stand rejected under 35 USC 103 as being unpatentable over Bacchetta in view of Wolf et al., "Silicon Processing for the VLSI Era, Vol. I: Process Technology." This rejection is respectfully traversed.

Claim 9 stands rejected under 35 USC 103 as being unpatentable over Bacchetta in view of Sung, U.S. Patent 6,235,592. This rejection is respectfully traversed.

Independent claim 1 of the present application recites a method for forming a passivation layer on a memory device with an interconnect structure thereon, comprising: providing a plurality of metal interconnect structures; forming a passivation structure over the plurality of metal interconnect structures, wherein the passivation structure comprises a first dielectric layer and a silicon-oxy-nitride (SiOxNy) layer; and forming a second dielectric layer over the surface of the silicon-oxy-nitride layer; wherein **the first dielectric is formed by depositing a HDP**

oxide over the interconnect structure with high density plasma chemical vapor deposition (HDPCVD), and **the thickness of the first dielectric layer is between 7000 to 10000Å** so as to **perform passivation function**.

In contrast, *Bacchetta et al.* discloses a method comprising: forming a substrate 6 of the circuit structure 7 (see col. 3, lines 55-17 & Fig. 2); forming a first oxynitride layer 1 completely over that structure 7 (see col. 5, lines 38-40 & Fig. 2); forming a SOG only in the deeper zones 4 so as to planarize the upper surface (see col. 5, lines 42-45 & Fig. 2); forming an oxide adhesion layer 2 of 350 Å thick over the portion of the first oxynitride layer 1 not covered by the SOG, and over the residual SOG (see col. 5, lines 45-47); and forming a second oxynitride layer 3 (see col. 5, line 48 & Fig. 2) and a top PSG layer 5 (see col. 5, lines 51-52 & Fig. 2), sequentially.

More specifically, *Bacchetta et al.* teaches and suggests that the oxide adhesion layer 2, which is relied on by the Examiner as being comparable to the first dielectric layer of the present invention, is disposed between the layers 1 and 3 and serves no passivation function (see col. 4, lines 9-10), but serves adhesion function only. This is in contrast with the present application, in which a first dielectric layer **performs passivation function**, as is recited in independent claim 1. It is respectfully submitted that *Bacchetta et al.* **teaches away** from the present application, and therefore independent claim 1, as well as its dependent claims, is neither anticipated nor rendered obvious by *Bacchetta et al.*

Thus, even if the teachings of *Bacchetta et al.*, *Wu* and/or *Higashitani* were combined, the combination would not result in the presently claimed invention.

In addition, the Examiner acknowledges that neither *Bacchetta et al., Wu* nor *Higashitani* disclose the thickness of the first dielectric layer being substantially between **7000 to 10000Å** so as to **perform passivation function**. The Examiner then alleges that discovering the optimum or workable ranges involves only routine skill in the art where the general conditions of a claim are disclosed in the prior art. However, *Bachetta et al* teaches that an oxide adhesion layer 2 of about 350 Å is formed over the portion of the first oxinitride layer not covered by the SOG, and over the residual SOG (see col. 5, lines 45-47). Thick oxide adhesion layer interposesd between layers 1 and 3 inevitably causes additional stress therebetween, which *Bacchetta et al.* tries to avoid. Accordingly, *Bachetta et al.* strongly suggests that the oxide adhesion layer 2 should be thin, its thickness dimension being preferably on the order of a few nanometers, specifically within the range of 5 to 50 nm (see col. 4, lines 9-13) . Thus, *Bacchetta et al.* **teaches away** from increasing the thickness of the oxide adhesion layer 2, which is relied on by the Examiner for teaching of the first dielectric layer of the present invention. Therefore, one skilled in the art would lack the motivation to discover optimum or workable ranges by increasing the thickness of the first dielectric layer, if he were to follow the teaching of *Bacchetta et al.* On the contrary, the present application discloses that the thickness of the first dielectric layer is substantially between **7000 to 10000Å,** as recited in independent claim 1, which is at least ten times more than the maximum thickness of oxide adhesion layer (e.g. 50 nm or 500 angstroms) suggested by *Bacchetta et al.*

Thus, even if the teachings of *Bacchetta et al., Wu* and *Higashitani* were combined, the combination would not result in the presently claimed invention.

Also, the Examiner acknowledges that *Bacchetta et al.* and *Wu* do not disclose the first dielectric being formed by depositing a HDP oxide over the interconnect structure with high density plasma chemical vapor deposition (HDPCVD), but alleges that it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the oxide layer of *Bacchetta* in view of *Wu* by HDPCVD, as taught by *Higashitani.* However, *Bacchetta et al* is from a very different technical field than that of *Higashitani et al. Bacchetta et al.* is related to a process for manufacturing a monolithic intergrated circuit which includes overlaid layers of dielectric materials (see col. 1, lines 12-15). In contrast, *Higashitani et al.* is related to isolating active region in the semiconductor device, and more particularly to shallow trench isolation (STI) process, local oxidation of silicon (LOCOS) isolation processes, and combinations thereof (see col. 1, lines 6-10). The technical fields of these two patents are different from each other, and from the present application. Accordingly, there would be no motivation to combination these references as proposed by the Examiner. Therefore, it would not be obvious to one of ordinary skill in the art at the time of the invention to combine references from two non-analogous arts.

The additional references to Wolf et al. and Sung fail to overcome the deficiencies of the primary references, as discussed above.

In view of the foregoing amendments and remarks, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the method of independent claim 1, and its dependent claims. Accordingly, reconsideration and withdrawal of the 35 USC 103 rejections are respectfully requested.

Applicants gratefully acknowledge that the Examiner considers claims 12-22 to be allowable. In view of the foregoing amendments and remarks, it is respectfully submitted that all claims should be in condition for allowance.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By _____

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